



# USB to ATA/ATAPI/SD/MMC Interface Controller

## 1 General Description

SN11020 provides a high-performance interface to bridge USB and ATA/ATAPI/SD/MMC compliance device. By providing a flexible and low cost single chip solution for applications intended to utilize the convenience of USB, it could be used to connect IDE hard disk, CD-ROM, CD-RW, Compact Flash card, MMC or SD memory card. The maximum supported serial clock in SD/MMC interface is 12MHz and supported block length is 2048 bytes. The external serial EEPROM gives users the flexibility to customize USB vendor ID and product ID for various version of products. With Sonix drivers, product with SN11020 can performs like two removable disks to Windows or Mac OS. In addition, SN11020 can be configured as a CF/ATA/ATAPI only device or SD/MMC only device by simply setting jumper pins.

## 2 Features

USB 1.1 compatible.

Support ATA/ATAPI, PIO mode 0

SD memory card specification 1.0 compatible.

MMC memory card specification 2.1.1 compatible.

SD/MMC serial clock rate is up to 12MHz.

Built-in FIFO for upstream and downstream data transfer.

Pin selectable bus-power or self-power.

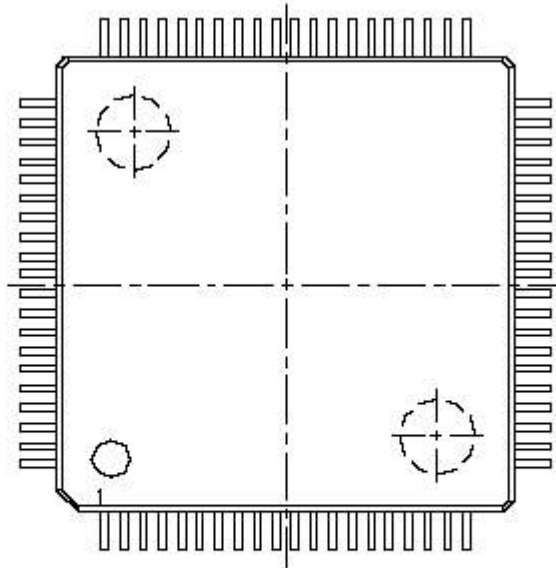
Eight user-defined general purpose IO.

Drivers support Microsoft Win 98/Win Me/Win 2000/Mac 8.6 ~ 9.x

Single 3.3V operation in 80-pin LQFP package.

### 3 Pin Assignment

#### 3.1 LQFP80 package



Pin#	Pin Name	Type	Drive	Special	Description
1	VSS	P	-	-	3.3V digital power ground
2	RSTN	DI		ST, PU	Bridge reset (internal pull-up)
3	TEST	DI		ST, PD	Test pin
4	SELPWR	DI		ST, PD	Power select pin; 0:Bus power 1: self power
5	GPIO0	DIO	8mA	ST, SR	General purpose input/output
6	GPIO1	DIO	8mA	ST, SR	General purpose input/output
7	GPIO2	DIO	8mA	ST, SR	General purpose input/output
8	GPIO3	DIO	8mA	ST, SR	General purpose input/output; input also used as USB wakeup
9	ATANIOR	DO	8mA	SR	ATAPI I/O read signal, active low
10	NC	-	-	-	No connected
11	NC	-	-	-	No connected



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12	ATANIOW	DO	8mA	SR	ATAPI I/O write signal, active low
13	ATADD3	DIO	8mA	TTL, SR	ATA data bit 3
14	ATADD11	DIO	8mA	TTL, SR	ATA data bit 11
15	ATADD4	DIO	8mA	TTL, SR	ATA data bit 4
16	ATADD12	DIO	8mA	TTL, SR	ATA data bit 12
17	ATADD5	DIO	8mA	TTL, SR	ATA data bit 5
18	ATADD13	DIO	8mA	TTL, SR	ATA data bit 13
19	ATADD6	DIO	8mA	TTL, SR	ATA data bit 6
20	VSS	P	-	-	3.3V digital power ground
21	NC	-	-	-	No connected
22	VDD	P	-	-	3.3V digital power supply
23	XVDD	P	-	-	Oscillator power supply
24	XIN	I	-	-	Crystal input or oscillator input
25	XOUT	O	-	-	Crystal output or no connection
26	XVSS	P	-	-	Oscillator power ground
27	ATADD14	DIO	8mA	TTL, SR	ATA data bit 14
28	ATADD7	DIO	8mA	TTL, SR	ATA data bit 7
29	VSS	P	-	-	3.3V digital power ground
30	ATADD15	DIO	8mA	TTL, SR	ATA data bit 15
31	NC	-	-	-	No connected
32	ATADD0	DIO	8mA	TTL, SR	ATA data bit 0
33	ATADD1	DIO	8mA	TTL, SR	ATA data bit 1
34	ATADD8	DIO	8mA	TTL, SR	ATA data bit 8
35	ATADD2	DIO	8mA	TTL, SR	ATA data bit 2
36	ATADD9	DIO	8mA	TTL, SR	ATA data bit 9
37	ATADD10	DIO	8mA	TTL, SR	ATA data bit 10
38	ATACS0	DO	8mA	SR	ATAPI chip select 0
39	VDD	P	-	-	3.3V digital power supply
40	NC	-	-	-	No connected
41	VSS	P	-	-	3.3V digital power ground
42	ATACS1	DO	8mA	SR	ATAPI chip select 1
43	ATADA2	DO	8mA	SR	ATAPI device address 2
44	ATADA1	DO	8mA	SR	ATAPI device address 1
45	ATADA0	DO	8mA	SR	ATAPI device address 0



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46	ATARSTN	DO	8mA	SR	ATA reset, active low
47	ATAIRDY	DI	-	TTL, ST	ATAPI data ready signal, active high
48	ATAINTR	DI	-	TTL, ST	ATA interrupt request
49	VDD	P	-	-	3.3V digital power supply
50	ROMDO	DI	-	ST	Serial data from external EEPROM
51	NC	-	-	-	No connected
52	NC	-	-	-	No connected
53	ROMSK	DO	4mA	SR	Clock for external serial EEPROM
54	ROMCS	DO	4mA	SR	Chip select for external EEPROM
55	SDDIO0	DIO	8mA	SR, ST	SD/MMC data 0
56	SDDIO1/ROMDI	DIO	8mA	SR, ST	SD data 1/ Serial data to external EEPROM
57	SDDIO2	DIO	8mA	SR, ST	SD data 2
58	SDDIO3	DIO	8mA	SR, ST	SD data 3
59	SDCMD	DIO	8mA	SR, ST	SD/MMC command
60	VSS	P	-	-	3.3V digital power ground
61	VDD	P	-	-	3.3V digital power supply
62	SDCLK	DO	8mA	SR	SD/MMC bus clock
63	PWRSW	DO	8mA	SR	Power down control
64	GPIO4	DIO	8mA	ST, SR	General purpose input/output
65	GPIO5	DIO	8mA	ST, SR	General purpose input/output
66	GPIO6	DIO	8mA	ST, SR	General purpose input/output; for SD, it is the write-protect pin
67	GPIO7	DIO	8mA	ST, SR	General purpose in/output; for SD, it is the card-detect pin
68	VSS	P	-	-	3.3V digital power ground
69	TAVDD	P	-	-	USB transceiver power supply
70	DPLUS	AIO	-	-	USB D+ signal
71	NC	-	-	-	No connected
72	NC	-	-	-	No connected



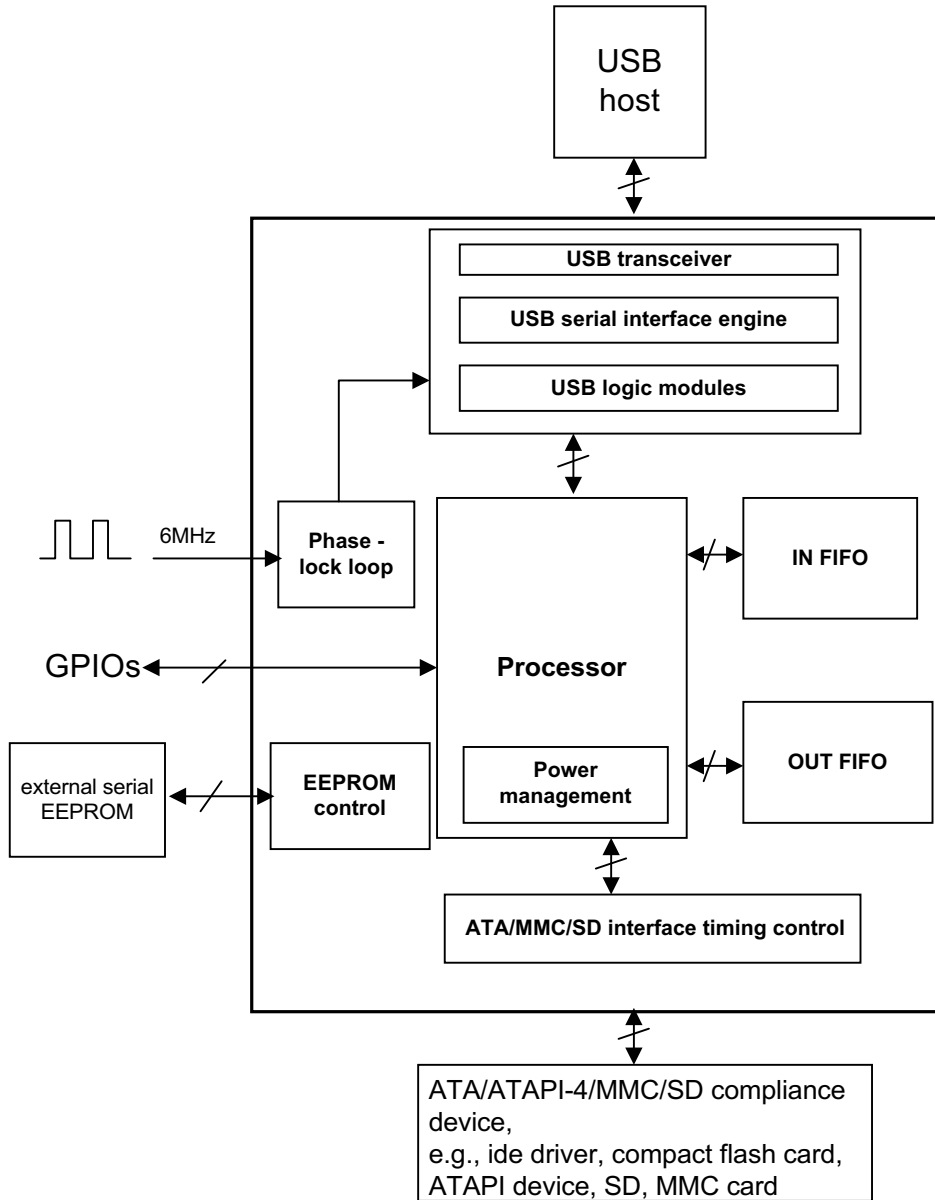
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73	NC	-	-	-	No connected
74	DMINUS	AIO	-	-	USB D- signal
75	TAVSS	P	-	-	USB transceiver power ground
76	AVSS	P	-	-	On-chip PLL power ground
77	AVDD	P	-	-	On-chip PLL power supply
78	VDD	P	-	-	3.3V digital power supply
79	NC	-	-	-	No connected
80	NC	-	-	-	No connected

- P: power pin; AI: analog input pin, AIO: analog input/output pin; DI: digital input pin; DO: digital output pin; DIO: digital input/output pin.
- TTL: TTL compatible input pin; ST: schmit trigger pad, PD: pull down; PU: pull up; SR: slew rate control.

## 4 Block Diagram





## 5 Electrical Characteristics

### 5.1 Absolute maximum rating

symbol	parameter	value	unit
DV <sub>min</sub>	min digital supply voltage	DGND – 0.3	V
DV <sub>max</sub>	max digital supply voltage	DGND + 4.6	V
AV <sub>min</sub>	min analog supply voltage	AGND – 0.3	V
AV <sub>max</sub>	max analog supply voltage	AGND + 4.6	V
DV <sub>inout</sub>	voltage on any digital input or output pin	DGND –0.3 to 5.5	V
AV <sub>inout</sub>	voltage on any analog input or output pin	AGND –0.3 to Av <sub>dd</sub> + 0.3	V
T <sub>A</sub>	storage temperature range	-40 to +125	C
ESD (HBM)	ESD human body mode	2000	V
ESD (MM)	ESD machine mode	200	V
I <sub>off</sub>	Leakage current	10	uA
I <sub>latch</sub>	Minimum latch up current	100	mA

### 5.2 Operation conditions

symbol	parameter	value	unit
DV <sub>dd</sub>	digital supply voltage	+3 to +3.6	V
Av <sub>dd</sub>	analog supply voltage	+3 to +3.6	V
T <sub>A</sub>	operating temperature range	0 to 70	C

### 5.3 AC electrical characteristics

symbol	parameter	value	unit
CLK <sub>in</sub>	system clock input to PLL	6 (typ)	MHz
	CLK <sub>in</sub> duty cycle	50 ± 2	%



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Fsk	SK pin clock frequency	200	kHz
Tsks	min setup time for DR to SK falling edge	20	ns
Tskh	min hold time for DR to SK falling edge	20	ns

## 5.4 DC electrical characteristics

Symbol	Parameter	Value	Unit
VIH	High level input current	$0.7 \cdot DV_{dd}$	V
VIL	Low level input current	$0.3 \cdot DV_{dd}$	V
VOH	High level output voltage	$0.7 \cdot DV_{dd}$	V
VOL	Low level output voltage	$0.3 \cdot DV_{dd}$	V